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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/766,896	01/22/2001	Hidemitsu Aoki	WAM-03401	2616	
75	90 05/28/2002				
Patent Group			EXAMINER		
Hutchins, Whee 101 Federal Str	eet		DEO, DU	DEO, DUY VU	
Boston, MA 02110			ART UNIT	PAPER NUMBER	
			1765	1765	
			DATE MAILED: 05/28/2002	DATE MAILED: 05/28/2002	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	09/766,896	AOKI ET AL.				
Office Action Summary	Examiner	Art Unit				
	DuyVu n Deo	1765				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status						
1) Responsive to communication(s) filed on 17.	<u> April 2002</u> .					
	nis action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims						
4)⊠ Claim(s) <u>1-29</u> is/are pending in the application.						
4a) Of the above claim(s) <u>1-8</u> is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>9-29</u> is/are rejected.						
7) Claim(s) is/are objected to.						
	laction requirement					
8) Claim(s) <u>1-8</u> are subject to restriction and/or election requirement. Application Papers						
9) The specification is objected to by the Examiner.						
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12)☐ The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)□ Some * c)□ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
 a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121. 						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2	5) Notice of Informal Pa	(PTO-413) Paper No(s) atent Application (PTO-152)				

Art Unit: 1765

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 9-29 in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

2. Claims 9-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9-26 recites "using the stripper compositions of claims 1-6," which have been restricted and withdrawn without traverse as stated above. Examiner suggests incorporating all the limitations of claims 1-6 into claims 9-26 respectively.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in-
- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
- (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).
- 4. Claims 9-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Small (US 5,981,454).

Application/Control Number: 09/766,896

Art Unit: 1765

12

Small describes a method for removal of chemical residues, which have been applied in a previous step, from the metal surface or dielectric surface of a semiconductor substrate using a solution comprising: gallic acid (hydroxyl aromatic compound), urea hydroperoxide (urea or an urea derivative), water, and hydroxylamine (col. 7, line 10, 35; col. 8, line 27; table III; claim 1).

The concentration of gallic acid, urea hydroperoxide, hydroxylamine, and water are 1-25 wt%, 0.5-30 wt%, 30 wt%, 5 wt% respectively (col. 7, line 22; col. 8, line 29; table III).

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 15-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Small and Zhao et al. (US 6,204,192).

Unlike claimed invention, Small is silent about prior steps of patterning the dielectric layer to expose the metal layer including steps of forming a metal film (copper), 1st dielectric film, and resist or 2nd dielectric film, etching the 1st dielectric layer using the resist film or 2nd dielectric layer as a mask to expose the metal layer. However, these steps are well known to one skill in the art as shown here by Zhao (fig. 2; col. 4). It would have been obvious to one skill in the art at the time of the invention that Small's method can be used in any semiconductor process, such as a single or dual damascene process taught by Zhao, that has dielectric and metal layer in order to clean the dielectric and metal layers with an expected result.

Application/Control Number: 09/766,896

Art Unit: 1765

7. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morinaga et al. (US 5,885,362).

Morinaga describes a method for cleaning semiconductor, metal, and glass surfaces using a solution comprising pyrogallol (hydroxy aromatic compound), urea and its derivatives, dimethylenethanolamine (alkanolamine), and water (col. 3, line 37-42; col. 5, line 10-12; col. 7, line 22; col. 8, line 34-40). Even though Morinaga doesn't describes stripping of resist or etching residues from the semiconductor substrate having exposed metal film. However, he teaches using the solution for cleaning/etching of semiconductor, metal, and glass surface (col. 13, line 55-63); therefore, it would have been obvious at the time of the invention for one skill in the art to use the solution in cleaning etching residues from the semiconductor wafer having exposed metal film in order to obtain a clean wafer with an expected result.

Referring to claim 11, the amount of each of compound in the solution would have been obvious to one skill in the art to be determined through test runs in order to achieve the optimum concentration of each compound in the solution to clean the wafer with an expected result. See in re Aller et al., 105 USPQ 233.

8. Claims 15-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morinaga and Zhao et al. (US 6,204,192).

Unlike claimed invention, Morinaga is silent about prior steps forming a semiconductor wafer including steps of forming a metal film (copper), 1st dielectric film, and resist or 2nd dielectric film; etching the 1st dielectric layer using the resist film or 2nd dielectric layer as a mask to expose the metal layer. However, these steps are well known to one skill in the art as shown here by Zhao (fig. 2; col. 4). It would have been obvious to one skill in the art at the time

Application/Control Number: 09/766,896

Art Unit: 1765

of the invention that Morinaga's method can be used in any semiconductor process, such as a

single or dual damascene process taught by Zhao, because Morinaga teaches that his solution can

be used to clean/etch semiconductor wafer and in order to clean semiconductor substrate with an

expected result.

9. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to DuyVu n Deo whose telephone number is 703-305-0515.

DVD

May 22, 2002

BENJAMIN L. UTECH SUPERVISORY PATENT EXAMINER

Page 5

TECHNOLOGY CENTER 1700